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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/338,286	06/22/1999	RICHARD SNOW	IGT1P073	1185

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BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY, CA 94704-0778

EXAMINER	
HOTALING, JOHN M	

ART UNIT	PAPER NUMBER
3713	

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/338,286	SNOW ET AL.
	Examiner	Art Unit
	John M Hotaling II	3713

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10,11,15,16 and 20-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *10,11,15,16 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 11, 15, 16, 20, 21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss US Patent 6,071,190 in view of Byers et al US Patent 5,788,509. The rejections contained in the previous office actions are relevant and incorporated herein. Weiss discloses all of the instant application without specifically disclosing how the various processing subsystems are connected such as the use of a motherboard with expansion slots and a serial UART. Weiss teaches a plurality of processors connected by a serial or parallel link or a motherboard with separate tasks performed whereby critical gaming functions may be partitioned from other functions by executing critical gaming functions on a separate dedicated processor and partitioning the devices hardware so that the functions not deemed critical which are stored or executed from alterable media are not capable of directly modifying the random access memory used by the critical gaming function. Further Weiss discloses in column 4 that any component required to be uniquely controlled by the critical gaming functions are preferably not accessible by other functions stored or executed from alterable media. Thus the non-alterable media containing the critical gaming functions is easily verifiable as to content independent of any function of the gaming device itself. In column 2 of

Weiss it is disclosed that a need exists for an independent secured processor design for validation which would provide all key functions such as the determination of game outcome, monetary input, output, and logging of relevant events. Furthermore, a need exists for an open architecture design, for example, a personal computer based design (with respect to claim 20) of the gaming device which would provide all shell functions of presenting the game environment and thus providing a substantial entertainment component of the gaming device. Weiss teaches that it is obvious to use a plurality of processing platforms constructed to be in communication with each other to provide security and be expandable for other gaming functions. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Weiss to connect the various processing systems such as by using a personal computer based design. With respect to claim 10 please see figure 2, figure 6 and column 6, 11, and 12 which disclose a housing 100, a plurality of user inputs, a display 50, a gaming processing subsystem is a secure processing area 60 which includes a processor board 162 and a main board 164 which controls the display and sound generated connected by a bus to a back plane 166. Board 164 also encompasses the general computing subsystem and has a bus interface and an expansion board. The processor board 162, a main board 164 and the back plane 166 may be integrally or separately formed. The main board includes memory in the form of ROM and EEPROM which can be non-volatile memory as disclosed in column 11. The use of PCI, ISA, VME, or AGP in order to connect peripherals to a bus are well known standards in the computing arts and will be treated as analogous interface protocols. With respect to claim 11 column 12 and

figure 7 disclose a second gaming processing subsystem board 252, furthermore, the first gaming processing subsystem board controls the one or more features as outlined above. With respect to claim 15, column 11 discloses serial interface for linking with a second processing area and figure 6 which discloses a back plane for connection to peripherals and a plurality of communication ports. With respect to claims 16, and 21-23 Weiss discloses in columns 11 and 12 that the main board 164 is connected to another board 162, in addition the main board has a random number generator associated with it, and the main board has a back plane 166 which is integrally or separately formed. The processor board also allows peripherals in the form of, for example, hard drives, CD ROMS, network interfaces, sound cards, and other desirable peripherals for game enhancement and patron entertainment. In an analogous invention to Byers et al teaches that it is known to attach to a motherboard Industry Standard Architecture (ISA) expansion cards that connect the computer electronics to the peripheral device. . With respect to claim 16 a PCI expansion card meets the definition of an ISA expansion card. Therefore, It would be obvious to one of ordinary skill in the art at the time of the invention to have a pc computer with a motherboard capable of accepting cards using the motivation provided by Weiss that a computer backplane could be integrally or separately formed on the main board (motherboard) and that other desired peripherals for game enhancement and patron entertainment could be added to the main board.

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss US Patent 6,071,190 in view of Byers et al US Patent 5,788,509 as applied to the claims above and further in view of Newtons Telecom Dictionary page 751 the definition of UART. Weiss and Byers discloses all of the instant application as disclosed above but lack in disclosing the specific use of a serial UART as disclosed in claims 22 and 23. Instead Weiss discloses that the processor board also allows peripherals in the form of, for example, hard drives, CD ROMS, network interfaces, sound cards, and other desirable peripherals for game enhancement and patron entertainment. In this case it would be obvious to one of ordinary skill in the art to use a UART for game enhancement since Weiss already uses serial and parallel communications and the a UART would be used in order to simplifiy those communications which are already part of a communication port.

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Hotaling II whose telephone number is 703 305 0780. The examiner can normally be reached on Mon-Thurs 7:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Teresa Walberg can be reached on (703) 308-1327. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JOHN M. HOTALING, II
PRIMARY EXAMINER

June 7, 2004